LSI/CSI

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LS7766

June 2012

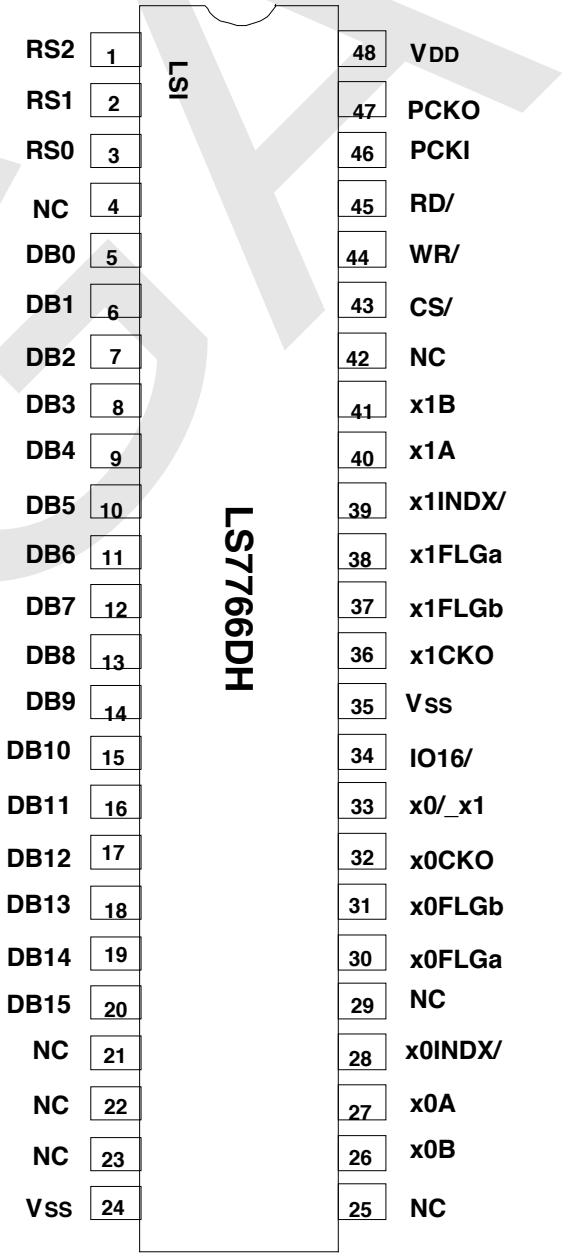
32-BIT SINGLE- AXIS/DUAL-AXIS QUADRATURE COUNTER

FEATURES:

- Direct interface with Incremental Encoders
- Read/write registers for count and I/O modes. Count modes include: non-quadrature (Up/Down), quadrature (x1, x2, x4.) free-run, non-recycle, modulo-n and range limit
- Programmable IOs for Index and Marker Flags
- Separate mode-control registers for each axis
- 40MHz count frequency at 5V; 20MHz count frequency at 3V
- Sets of 32-bit counters, input registers, output registers, comparators and 8-bit Status registers for each axis
- Digital filtering of the input quadrature clocks for noise immumity.
- Pin selectable 3-state 16-bit / 8-bit bus
- 3V to 5.5V operating voltage range
- Available in four different configurations identified by the following suffixes:
  DH = Dual-axis with pin selectable 16-bit/8-bit IO Bus
  DO = Dual-axis 8-bit IO Bus
  SH = Single-axis pin selectable 16-bit/8-bit IO Bus
  SO = Single axis 8-bit IO Bus
  LS7766DH-TS; LS7766DO, LS7766DO-S, LS7766DO-TS; LS7766SO, LS7766SO-S, LS7766SO-TS; LS7766SH-TS
  P/N = DIP; P/N-**S = SOIC**; **P/N-TS = TSSOP**

GENERAL DESCRIPTION:

The LS7766 consists of two identical modules of 32-bit programmable up/down counters (CNTR) with direct interface to incremental encoders. The modules can be configured to operate as quadrature-clock counters or non-quadrature up/down counters. In both quadrature and non-quadrature modes, the modules can be further configured into free-running, non-recycle, modulo-n and range-limit count modes. The mode configuration is made via two 8-bit read/write addressable mode control registers, MCR0 and MCR1. Data can be written into a 32-bit input data register (IDR), organized in addressable Word segments using the 16-bit IO bus or in byte segments using the 8-bit IO Bus. The IDR can be used to store target encoder positions and compared with the CNTR for generating marker flags when the CNTR reaches the target value. A 32-bit digital comparator is included for monitoring the equality of the CNTR to the IDR. Snapshots of the CNTR value can be stored in a read-addressable 32-bit output data register (ODR). The ODR can be read in Word segments or byte segments in accordance with the selected bus width. Data transfers among the registers and various register reset functions are performed by means of a write-addressable 8-bit transfer control register (TCR). A read-addressable 8-bit status register (STR), stores the count related status information such as CNTR overflow, underflow, count direction, etc.June



Pin Assignment - Top View

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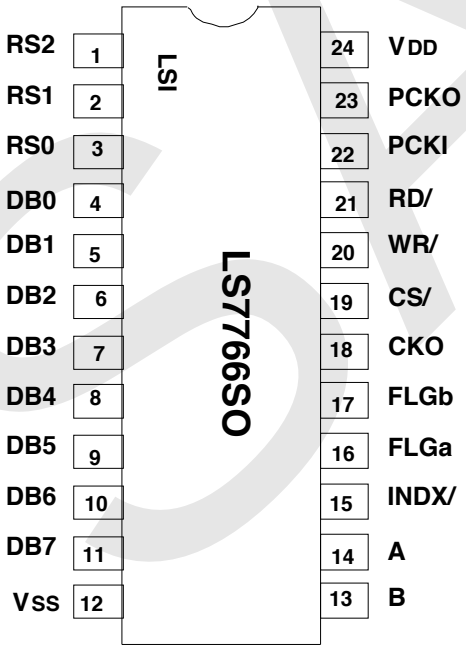
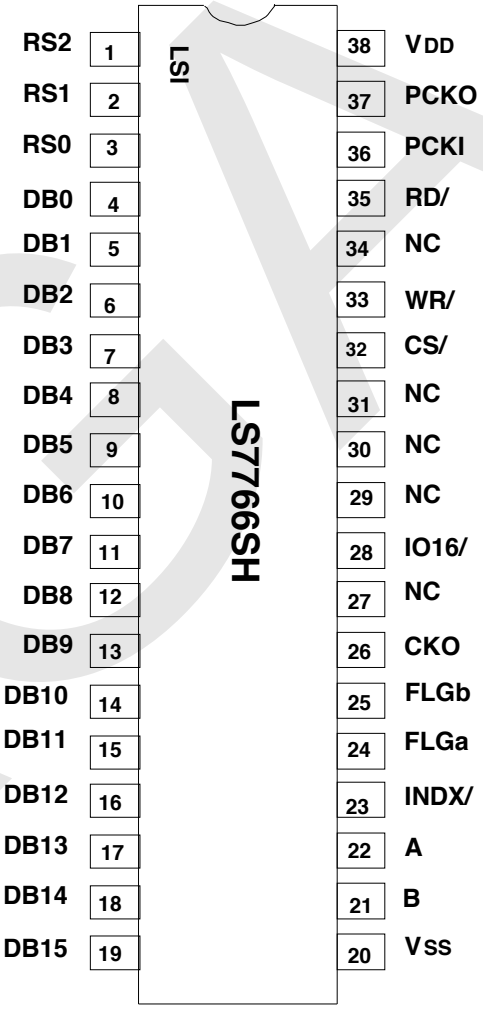


Pin Assignment - Top View



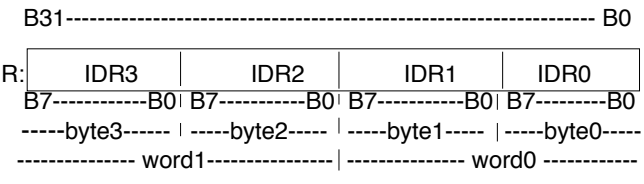
Pin Assignment - Top View

REGISTER DESCRIPTION:

Following is a list of the hardware registers for the single-axis device. For the dual axis device, these registers are duplicated for the second axis.

IDR

The IDR is a 32-bit data register directly addressable for write. In the 8-bit bus-configuration, the input data is written in byte segments of byte0 (IDR0), byte1 (IDR1), byte2 (IDR2) and byte3 (IDR3). In the 16-bit bus-configuration the data is written in word segments of word0 (IDR1:IDR0) and word1 (IDR3:IDR20).



The IDR serves as the input portal for the counter (CNTR) since the CNTR is not directly addressable for either read or write. In order to preset the CNTR to any desired value the data is first written into the IDR and then transferred to the CNTR.

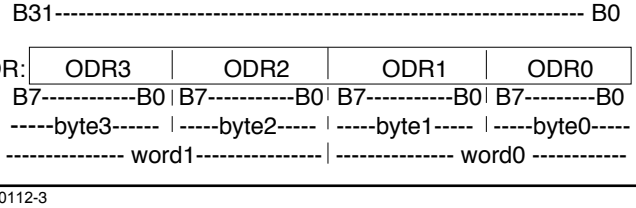
In **mod-n** and **range-limit** count modes the IDR serves as the repository for the division factor n and the count range-limit, respectively. The IDR can also be used to hold a target position data for comparing with the running CNTR. A compare equality flag is generated at IDR = CNTR to signal the event of arriving at the target.

CNTR:

The CNTR is a 32-bit up/down counter which counts the up/down pulses resulting from the quadrature clocks applied at A and B inputs or alternatively, in non-quadrature mode, pulses applied at the A input. The CNTR is not directly accessible for read or write; instead it can be preloaded with data from the IDR or it can port its own data out to the ODR which in turn can be accessed by read operation. In both quadrature and non-quadrature modes, the CNTR can be further configured into either free-running or single-cycle or mod-n or range-limit mode. In quadrature mode, the count resolution is programmable to be x1 or x2 or x4 of the A quad B cycles.

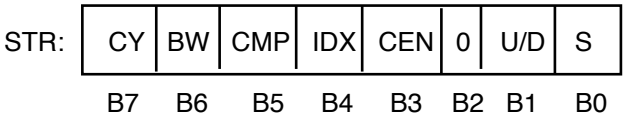
ODR:

The ODR is a 32-bit data register directly addressable for read. In the 8-bit bus-configuration, the output data is read in byte segments of byte0 (ODR0), byte1 (ODR1), byte2 (ODR2), and byte3 (ODR3). In the 16-bit bus configuration the data is read in word segments of word0 (ODR1:ODR0) and word1 (ODR3:ODR2).



STR:

The STR is an 8-bit status register indicating count related status.

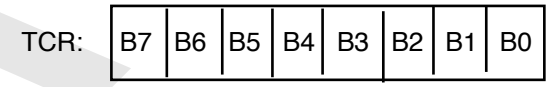


An individual STR bit is set to 1 when the bit related event has taken place. The STR is cleared to 0 at power-up. The STR can also be cleared through the control register TCR with the exception of bit_1(U/D) and bit3_(CEN). These two STR bits always indicate the instantaneous status of the count_direction and count_enable assertion/de-assertion. The STR bits are described below:

B7 (CY): Carry; set by CNTR overflow
B6 (BW): Borrow; set by CNTR underflow
B5 (CMP): Set when CNTR = PR
B4 (IDX): Set when INDX input is at active level
B3 (CEN): Set when counting is enabled,
reset when counting is disabled
B2 (0): Always 0
B1 (U/D): Set when counting up,
reset when counting down
B0 (S): Sign of count value;
set when negative, reset when positive

TCR:

The TCR is a write only register, which when written into, generates transient signals to perform load and reset operations as described below:



B0 = 0: Nop
= 1: Reset CNTR to 0.
(Should not be combined with
load_CNTR operation).
B1 = 0: Nop
= 1: Load CNTR from IDR. Affects all 32 bits.
(Should not be combined with
reset_CNTR operation)
B2 = 0: Nop
= 1: Load ODR from CNTR. Affects all 32 bits.
B3 = 0: Nop
= 1: Reset STR.
Affects status bits for carry, borrow, compare and index. Status bits corresponding to count_enable, count direction and sign are not affected
B4 = 0: Nop.
1: Master reset. Resets MCR0, MCR1, IDR, ODR, STR
B5 = 0: Nop
1: Set sign bit (STR bit0)
B6 = 0: Nop
1: Reset sign bit (STR bit0)
B7 = x: Not used.

MCR0 : The MCR0 is an 8-bit read/write register which configures the counting modes and the index input functionality. Upon power-up, the MCR0 is cleared to zero.

MCR0:	B7	B6	B5	B4	B3	B2	B1	B0

B1B0 = 00: Non-quadrature count mode (A = clock, B = direction).
= 01: x1 quadrature count mode (one count per quadrature cycle).
= 10: x2 quadrature count mode (two counts per quadrature cycle).
= 11: x4 quadrature count mode (four counts per quadrature cycle).
B3B2 = 00: **Free-running** count mode.
= 01: **Single-cycle** count mode (CNTR disabled with **carry** and **borrow**, re-enabled with **reset** or **load**)
= 10: **Range-limit** count mode (up and down count ranges are limited between IDR and zero, respectively. Counting freezes at these limits but resumes when the direction is reversed)
= 11: **Modulo-n** count mode (input count clock frequency is divided by a factor of [n+1], where n = IDR. In up direction, the CNTR is **cleared** to 0 at CNTR = IDR and up count continues. In down direction, the CNTR is **preset** to the value of IDR at CNTR = 0 and down count continues. A mod-n rollover marker pulse is generated at each limit at the FLGa output).
B5B4 = 00: Disable INDX/ input.
= 01: Configure INDX/ input as the load_CNTR input (transfers IDR to CNTR).
= 10: Configure INDX/ as the reset _CNTR input (clears CNTR to 0).
= 11: Configure INDX/ as the load_ODR input (transfers CNTR to ODR).
B6 = 0: Asynchronous index.
= 1: Synchronous index (overridden in non-quadrature mode).
B7 = 0: Input filter clock (PCK) division factor = 1. Filter clock frequency = f_{PCK}.
= 1: Input filter clock division factor = 2. Filter clock frequency = $f_{PCK}/2$.

MCR1: The MCR1 is an 8-bit read/write register which configures the FLGa and FLGb output functionality. In addition, the MCR1 can be used to enable/disable counting.Upon power-up, the MCR1 is cleared to zero:

MCR1:	B7	B6	B5	B4	B3	B2	B1	B0

B0 = 1: Enable Carry on FLGa (flags CNTR overflow; latched or unlatched logic low on carry).
B1 = 1: Enable Borrow on FLGa (flags CNTR underflow, latched or unlatched logic low on borrow).
B2 = 1: Enable Compare on FLGa (In free-running count mode a latched or unlatched logic low is generated in both up and down count directions at CNTR = IDR. In contrast, in range-limit and mod-n count modes a latched or unlatched low is generated at CNTR = IDR in the up-count direction only.
B3 = 1: Enable index on FLGa (flags index, latched or unlatched logic low when INDX input is at active level)
B5B4 = 00: FLGb disabled (fixed high)
= 01: FLGb = **Sign**, high for negative signifying CNTR underflow, low for positive.
= 10: FLGb = **Up/Down** count direction, high in count-up, low in count-down.
B6 = 0: Enable counting.
= 1: Disable counting.
B7 = 0: FLGa is latched.
= 1: FLGa is non-latched and instantaneous.

NOTE: Carry, Borrow, Compare and Index can all be simultaneously enabled on FLGa.

I/O PINS: The following is a description of the input/out pins.

RS0, RS1, RS2
Inputs. These three inputs select the hardware registers for read/write access according to Table 1 and Table 2. Table 1 applies to 8-bit bus configuration. Table 2 applies to 16-bit bus configuration.

TABLE 1

CS/	RS2	RS1	RS0	RD/	WR/	SELECTED REGISTER	DATABUS REGISTER MAP	OPERATION
1	x	x	x	x	x	none	none	none
0	0	0	0	0	1	MCR0	DBL	READ
0	0	0	1	0	1	MCR1	DBL	READ
0	0	1	0	0	1	ODR0	DBL	READ
0	0	1	1	0	1	ODR1	DBL	READ
0	1	0	0	0	1	ODR2	DBL	READ
0	1	0	1	0	1	ODR3	DBL	READ
0	1	1	0	0	1	STR	DBL	READ
0	0	0	0	1	0	MCR0	DBL	WRITE
0	0	0	1	1	0	MCR1	DBL	WRITE
0	0	1	0	1	0	IDR0	DBL	WRITE
0	0	1	1	1	0	IDR1	DBL	WRITE
0	1	0	0	1	0	IDR2	DBL	WRITE
0	1	0	1	1	0	IDR3	DBL	WRITE
0	1	1	0	1	0	TCR	DBL	WRITE

TABLE 2

CS/	RS2	RS1	RS0	RD/	WR/	SELECTED REGISTER	DATABUS REGISTER MAP	OPERATION
1	x	x	x	x	x	none	none	none
0	0	0	0	0	1	[MCR1:MCR0]	[DBH:DBL]	READ
0	0	1	0	0	1	[ODR1:ODR0]	[DBH:DBL]	READ
0	1	0	0	0	1	[ODR3:ODR2]	[DBH:DBL]	READ
0	1	1	0	0	1	[STR]	[DBL]	READ
0	0	0	0	1	0	[MCR1:MCR0]	[DBH:DBL]	WRITE
0	0	1	0	1	0	[IDR1:IDR0]	[DBH:DBL]	WRITE
0	1	0	0	1	0	[IDR3:IDR2]	[DBH:DBL]	WRITE
0	1	1	0	1	0	[TCR]	[DBL]	WRITE

Note 1. x indicates don't care case.

Note 2. DBL stands for DB <7:0> ; DBH stands for DB <15:8>.

x0/_x1 Input. The x0/_x1 input selects between axis-0 and axis-1 for Read and Write operations. A low at this input selects axis-0 while a high selects axis-1.

RD/ Input. A low on RD/ input accesses an addressed register(s) for read and places the data on the databus, DB<15:0> in accordance with Table 1 and Table 2.

CS/ Input. A low on the CS/ input enables the chip for read or write operation. When the CS/ input is high, read and write operations are disabled and the databus, DB<15:0> is placed in a high impedance state.

WR/ Input. A low pulse on the WR/ input writes the data on the databus, DB<15:0> into the addressed register according to Table 1 and Table 2. The write operation is completed at the trailing edge of the WR/ pulse.

PCKI, PCKO. Input, Output. A clock applied at PCKI input is used for validating the logic states of the A and B quadrature clocks and the INDX/ input. Alternatively, a crystal oscillator connected between PCKI and PCKO can be used to generate the filter clock.
The PCK input frequency, f_{PCK} is divided down by a factor of 1 or 2 according to bit7 of MCR0. The resultant clock is used to sample the logic levels of the A, the B and the INDX inputs. If a logic level at any of these inputs remains stable for a minimum of two filter clock periods, it is validated as a correct logic state.

The PCKI input is common to both axes, but the filter clock frequency for any axis is set by its associated MCR0 register.

In non-quadrature mode, no filter clock is used and the PCKI input should be connected to either V_{DD} or GND.

x0A, x0B Inputs. These are the A and B count inputs in axis-0. These inputs can be configured to function either in quadrature mode or in non-quadrature mode. The configuration is made through MCR0. In quadrature mode, A and B clocks are 90 degrees out of phase such as the output from an Incremental Encoder. When A leads B in phase, the CNTR counts up and when B leads A in phase, the CNTR counts down.

In non-quadrature mode, A serves as the count input while B controls the count direction. When B is **high**, positive transitions at the A input causes the CNTR to count **up**. Conversely, when B is **low**, the positive transition at the A input causes the CNTR to count **down**.

In quadrature mode, A and B inputs are sampled by an internal filter clock generated from the PCKI input. In non-quadrature mode, A and B inputs are not sampled and the count clocks are applied to the CNTR, bypassing the filter circuit.

x1A , **x1B**:
These are the A and B inputs corresponding to axis-1, . Functionally, they are identical with the A and B inputs of axis-0.

x0INDX/ Input. The INDX/ input in axis-0. The INDX/ input can be configured to function as load_CNTR or reset_CNTR or load_ODR input via MCR0. In quadrature mode the INDX/ input can be configured to operate in either synchronous or asynchronous mode. In the synchronous mode the INDX/ input is sampled with the same filter clock used for sampling the A and the B inputs and must satisfy the phase relationship with A and B in which INDX/ is at the active level during a minimum of a quarter cycle of both A and B high or both A and B low. The active level of the INDX/ input is logic low.

In non-quadrature mode the INDX/ input is unconditionally set to the asynchronous mode. In the asynchronous mode the INDX/ input is not sampled and can be applied in any phase relationship with respect to the A and B inputs.

The INDX/ input can be either enabled or disabled in both quadrature and non-quadrature modes.

x1INDX/. The INDX/ input corresponding to axes-1. Functionally, it is identical with the INDX/ input of axis-0.

IO16/ Input. When low, 16-bit databus configuration is invoked in accordance with Table 2. When high, 8-bit databus configuration is invoked in accordance with Table 1. This input has an internal pull-up.

x0FLGa Output. The FLGa output in axis-0. The FLGa output is configured by MCR1 register to function as Carry and/or Borrow and/or Compare and/or Index flag. A Carry flag is generated when the CNTR overflows, a Borrow flag is generated when the CNTR underflows, a Compare flag is generated by the condition, CNTR = IDR and Index flag is generated when Index input is at active level. The FLGa output can be configured to produce outputs in either latched mode or instantaneous mode. In the latched mode when the selected event of Carry or Borrow or Compare or index has taken place, FLGa switches low and remains low until the status register, STR is cleared. In the instantaneous mode, a negative pulse is generated instantaneously when the event takes place. The FLGa output can be disabled to remain at a fixed logic high.

x1FLGa Output. The FLGa output corresponding to axes-1. Functionally, it is identical with the FLGa output of axis-0.

x0FLGb Output. The FLGb output in axis-0. The FLGb output is configured by MCR1 to function as either Sign or Up/Down count direction indicator.

When configured as Sign, the FLGb output remains high when CNTR is in an underflow state (caused by down counts at or below zero), indicating a negative number. When the CNTR counts up past zero, FLGb switches low, indicating a positive number.

When configured as Up/Down indicatior, a high at the FLGb indicates that the current count direction is up (incremental) whereas a low indicates that the direction is down or decremental.

The FLGb output can be disabled to remain at a fixed logic high.

x1FLGb Output**.** The FLGb output of axis-1. Functionally, it is identical with the FLGb output of axis-0.

x0CKO Output**.** Axis-0 count clock output. In non-quadrature mode, the CKO output is identical with the input-A clock. In quadrature mode, CKO is derived from the filtered and decoded quadrature clocks applied at the A and B inputs. In either mode CKO is a true representative of the internal count clock.

x1CKO Output**.** Axis-1 count clock output. Functionally, it is identical with the CKO output of axis-0.

V_{DD}. Supply voltage. Positive terminal.

GND. Supply voltage. Negative terminal.

Absolute Maximum Ratings:

Parameter	Symbol	Values	Unit
Voltage at any input	V_{IN}	V_{SS} - 0.3 to V_{DD} + 0.3	V
Supply Voltage	V_{DD}	+7.0	V
Operating Temperature	T_A	-25 to +80	^oC
Storage Temperature	T_{STG}	-65 to +150	^oC

DC Electrical Characteristics. (T_A = -25^{o}C to +80^{o}C, V_{DD} = 3V to 5.5V)

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Supply Voltage	V_{DD}	3.0	5.5	V	-
Supply Current	I_{DD}	-	800	μA	All clocks off
Input Logic Low	V_{IL}	-	0.15V_{DD}	V	-
Input Logic High	V_{IH}	0.5V_{DD}	-	V	-
Input Leakage Current	I_{ILK}	-	30	nA	-
Data Bus Leakage Current	I_{DLK}	-	60	nA	Data bus off
Data Bus Source Current	I_{DBH}	2.0	-	mA	V_O = V_{DD} - 0.5V, V_{DD} = 5V
Data Bus Sink Current	I_{DBL}	-6.0	-	mA	V_O = 0.5V, V_{DD} = 5V
FLGa, FLGb, INT/ Source	I_{OSRC}	1.0	-	mA	V_O = V_{DD} - 0.5V, V_{DD} = 5V
FLGa, FLGb, INT/ Sink	I_{OSNK}	-6.0	-	mA	V_O = 0.5V, V_{DD} = 5V

Transient Characteristics. (T_A = -25^o to +80^{o}C, V_{DD} = 3V to 5.5V)

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Read Cycle (See Fig. 2)					
RD/ Pulse Width	t_{r1}	80	-	ns	-
CS/ Set-up Time	t_{r2}	80	-	ns	-
CS/ Hold Time	t_{r3}	0	-	ns	-
RS<2:0> Set-up Time	t_{r4}	80	-	ns	-
RS<2:0> Hold Time	t_{r5}	10	-	ns	-
x0/_x1 Set-up Time	t_{r6}	80	-	ns	-
x0/_x1 Hold Time	t_{r7}	10	-	ns	-
DB<15:0> AccessTime	t_{r8}	80	-	ns	Access starts when both RD/ and CS/ are low.
DB<15:0> Release Time	t_{r9}	-	35	ns	Release starts when either RD/ or CS/ is terminated.
Back to Back Read delay	t_{r10}	10	-	ns	-
Write Cycle (See Fig. 3)					
WR/ Pulse Width	t_{w1}	45	-	ns	-
CS/ Set-up Time	t_{w2}	45	-	ns	-
CS/ Hold Time	t_{w3}	0	-	ns	-
RS<2:0> Set-up Time	t_{w4}	45	-	ns	-
RS<2:0> Hold Time	t_{w5}	10	-	ns	-
x0/_x1 Set-up Time	t_{w6}	45	-	ns	-
x0/_x1 Hold Time	t_{w7}	10	-	ns	-
DB<15:0> Set-up Time	t_{w8}	45	-	ns	-
DB<15:0> Hold Time	t_{w9}	10	-	ns	-
Back to Back Write Delay	t_{w10}	90	-	ns	-

For V_{DD} = 3.3V ±10%

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Quadrature Mode (See Fig. 4 - 6)					
PCKI High Pulse Width	t_1	24	-	ns	-
PCKI Low Pulse Width	t_2	24	-	ns	-
PCKI Frequency	f_{pCK}	-	20	MHz	-
Filter Clock (ff) Period	t_3	50	-	ns	$t_3 = t_1 + t_2$, MDR0 <7> = 0
	t_3	100	-	ns	$t_3 = t_1 + t_2$, MDR0 <7> = 1
Filter Clock frequency	f_f	-	20	MHz	$f_f = 1/t_3$
Quadrature Separation	t_4	52	-	ns	$t_4 > t_3$
Quadrature Clock Pulse Width	t_5	105	-	ns	$t_5 > 2t_3$
Quadrature Clock frequency	f_{QA}, f_{QB}	-	4.5	MHz	$f_{QA} = f_{QB} < 1/4t_3$
Quadrature Clock to Count Delay	t_{Q1}	$4t_3$	$5t_3$	-	-
x1, x2, x4 Count Clock Pulse Width	t_{Q2}	25	-	ns	$t_{Q2} = t_3/2$
Quadrature Clock to FLGa delay	t_{fda}	$4.5t_3$	$5.5t_3$	ns	-
Quadrature Clock to FLGb delay	t_{fdb}	$3t_3$	$4t_3$	ns	-
INDX/ Input Pulse Width	t_{id}	60	-	ns	$t_{id} > t_4$
INDX/ set-up time	t_{is}	10	-	ns	-
INDX/ hold time	t_{ih}	10	-	ns	-
FLGa Output Width	t_{fw}	50	-	ns	$t_{fw} \approx t_4$
Non-Quadrature Mode (See Fig. 7 - 8)					
Clock A - High Pulse Width	t_6	24	-	ns	-
Clock A - Low Pulse Width	t_7	24	-	ns	-
Direction Input B Set-up Time	t_{8s}	24	-	ns	-
Direction Input B Hold Time	t_8	20	-	ns	-
Clock Frequency	f_A	-	20	MHz	$f_A = (1/(t_6 + t_7))$
Clock to FLGa Out Delay	t_9	-	40	ns	-
FLGa Out Pulse Width	t_{10}	24	-	ns	$t_{10} = t_7$
INDX/ Pulse Width	t_{11}	30	-	ns	-

For V_{DD} = 5V ±10%

Parameter	Symbol	Min. Value	Max.Value	Unit	Remarks
Quadrature Mode (See Fig. 4 - 6)					
PCK High Pulse Width	t_1	12	-	ns	-
PCK Low Pulse Width	t_2	12	-	ns	-
PCK frequency	f_{pCK}	-	40	MHz	-
Filter Clock (ff) period	t_3	25	-	ns	$t_3 = t_1 + t_2$, MDR0 <7> = 0
	t_3	50	-	ns	$t_3 = t_1 + t_2$, MDR0 <7> = 1
Filter Clock frequency	f_f	-	40	MHz	-
Quadrature Separation	t_4	26	-	ns	$t_4 > t_3$
Quadrature Clock Pulse Width	t_5	52	-	ns	$t_5 > 2t_3$
Quadrature Clock frequency	f_{QA}, f_{QB}	-	9.6	MHz	$f_{QA} = f_{QB} < 1/4t_3$
Quadrature Clock to Count Delay	t_{Q1}	$4t_3$	$5t_3$	-	-
x1, x2, x4 Count Clock Pulse Width	t_{Q2}	12	-	ns	$t_{Q2} = t_3/2$
Quadrature Clock to FLGa delay	t_{fda}	$4.5t_3$	$5.5t_3$	ns	-
Quadrature Clock to FLGb delay	t_{fdb}	$3t_3$	$4t_3$	ns	-
INDX/ Input Pulse Width	t_{id}	32	-	ns	$t_{id} > t_4$
INDX/ set-up time	t_{is}	5	-	ns	-
INDX/ hold time	t_{ih}	5	-	ns	-
FLGa Output Width	t_{fw}	24	-	ns	$t_{fw} \approx t_4$
Non-Quadrature Mode (See Fig. 7 - 8)					
Clock A - High Pulse Width	t_6	12	-	ns	-
Clock A - Low Pulse Width	t_7	12	-	ns	-
Direction Input B Set-up Time	t_8	12	-	ns	-
Direction Input B Hold Time	t_8	10	-	ns	-
Clock frequency	f_A	-	40	MHz	$f_A = (1/(t_6 + t_7))$
Clock to FLGa Out Delay	t_9	-	20	ns	-
FLGa Out Pulse Width	t_{10}	12	-	ns	$t_{10} = t_7$
INDX/ Pulse Width	t_{11}	15	-	ns	-

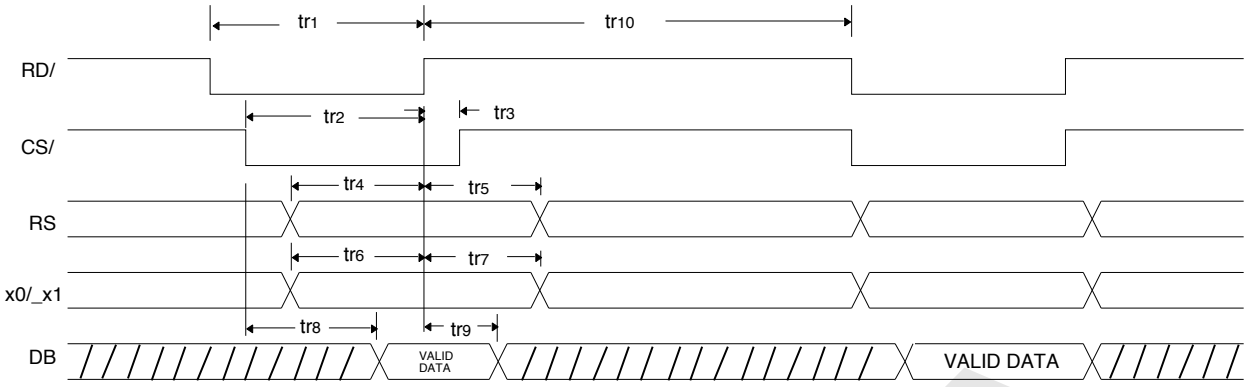


FIGURE 2. READ CYCLE

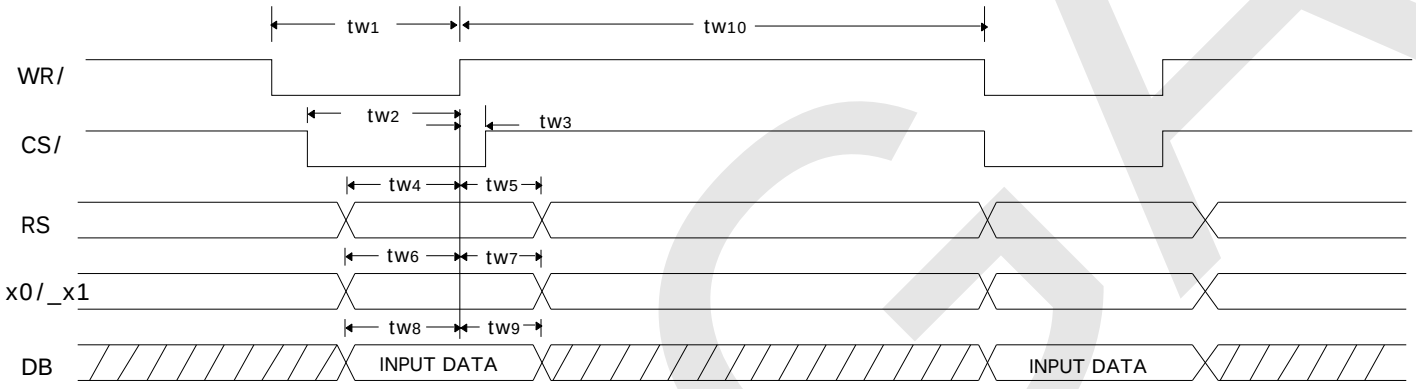
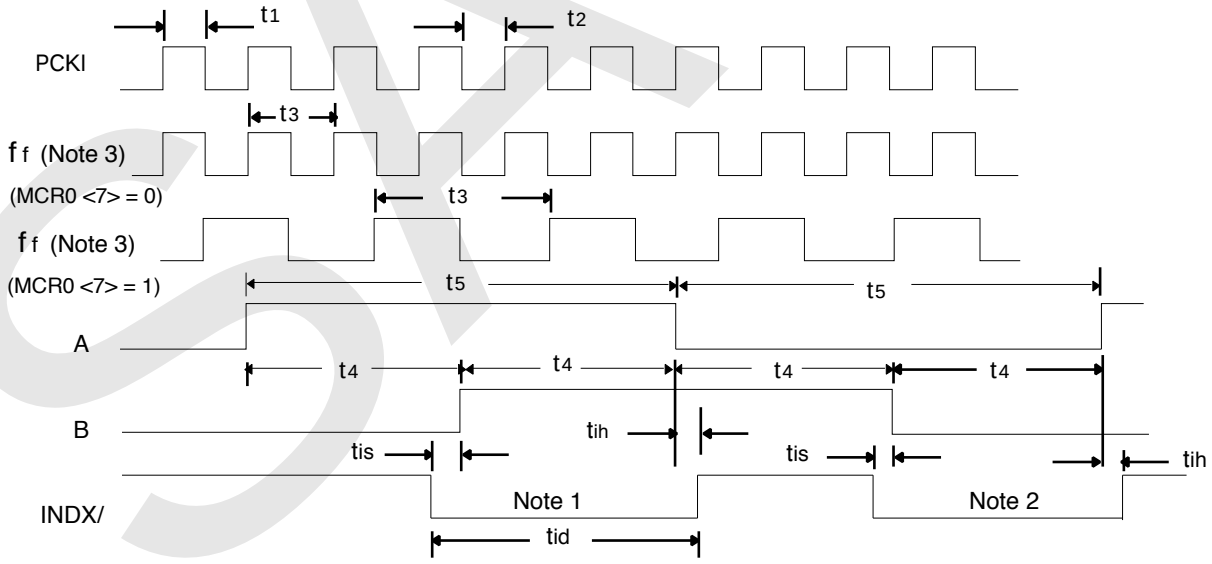
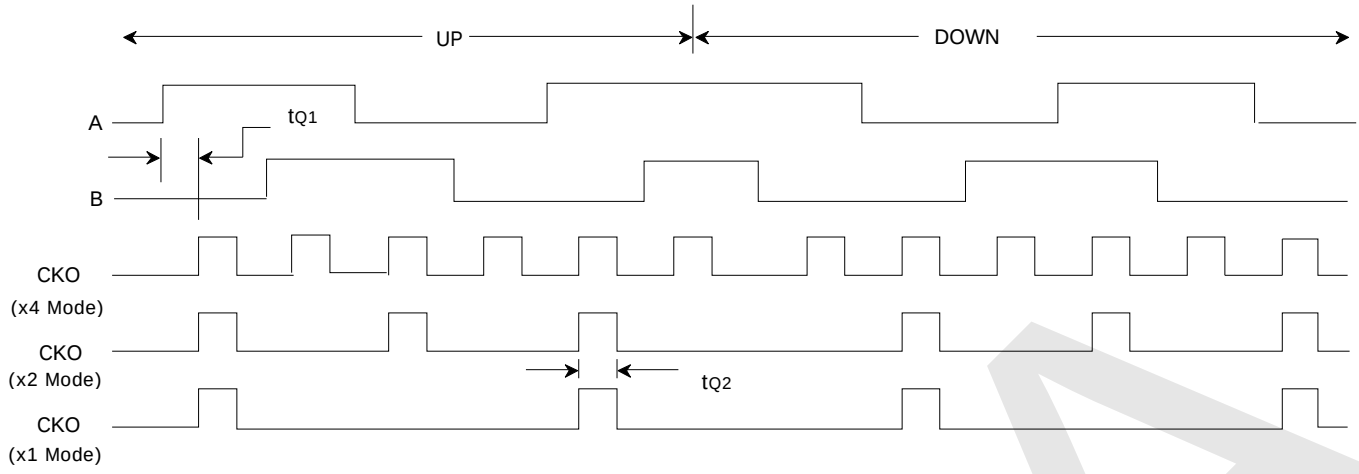


FIGURE 3. WRITE CYCLE



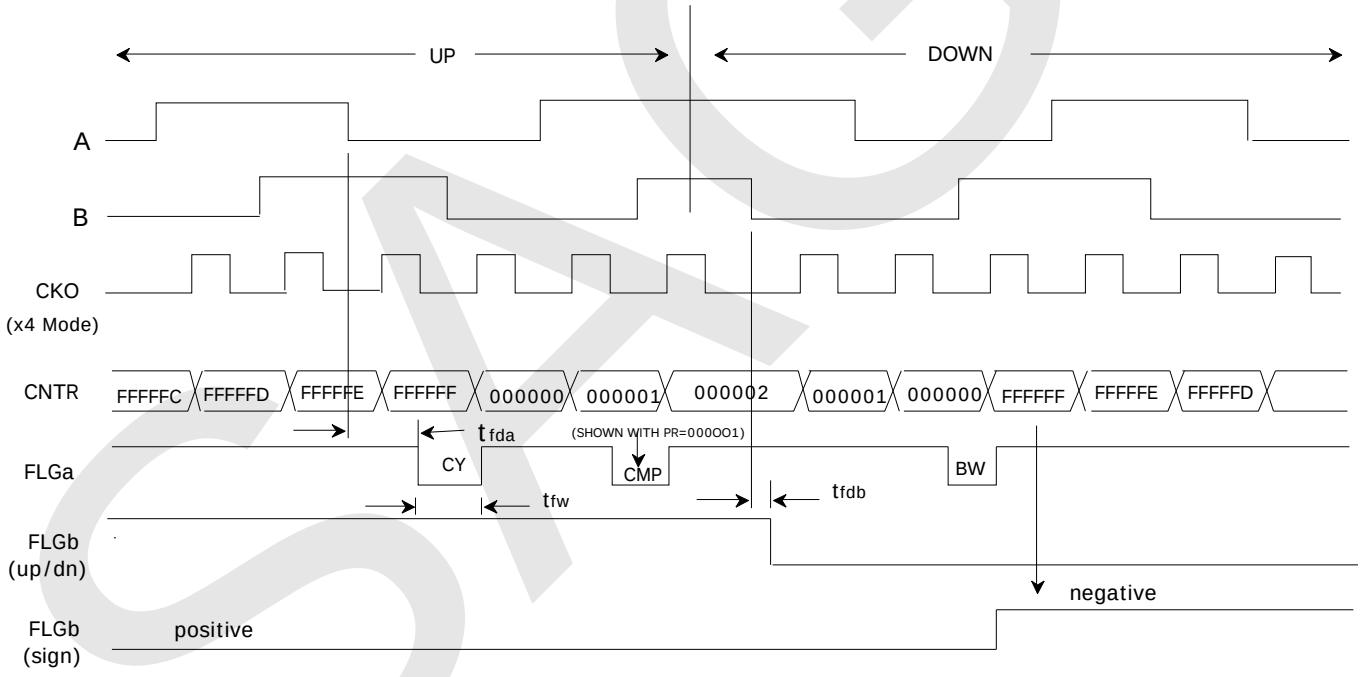
Note 1. Synchronous mode index coincident with both A and B high.
Note 2. Synchronous mode index coincident with both A and B low.
Note 3. f_F is the internal effective filter clock.

FIGURE 4. PCKI, A, B AND INDX/



NOTE. CKO is identical with internal count clock.

FIGURE 5. A/B QUADRATURE CLOCKS vs OUTPUT CLOCK, CKO



NOTE. FLGa is in non-latched mode.

FIGURE 6. QUADRATURE CLOCKS vs FLGa, FLGb OUTPUTS

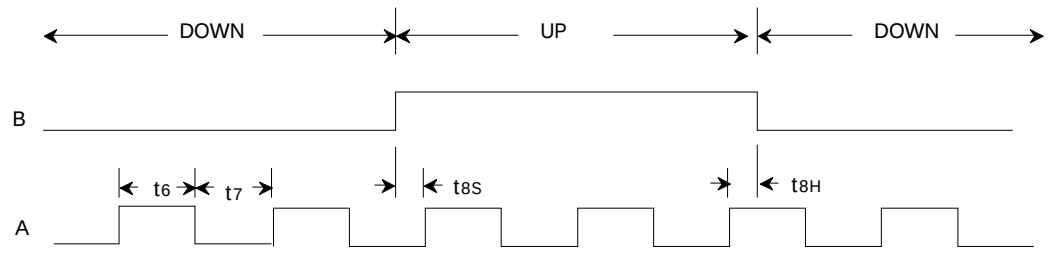


FIGURE 7. COUNT (A) AND DIRECTION (B) INPUTS IN NON-QUADRATURE MODE

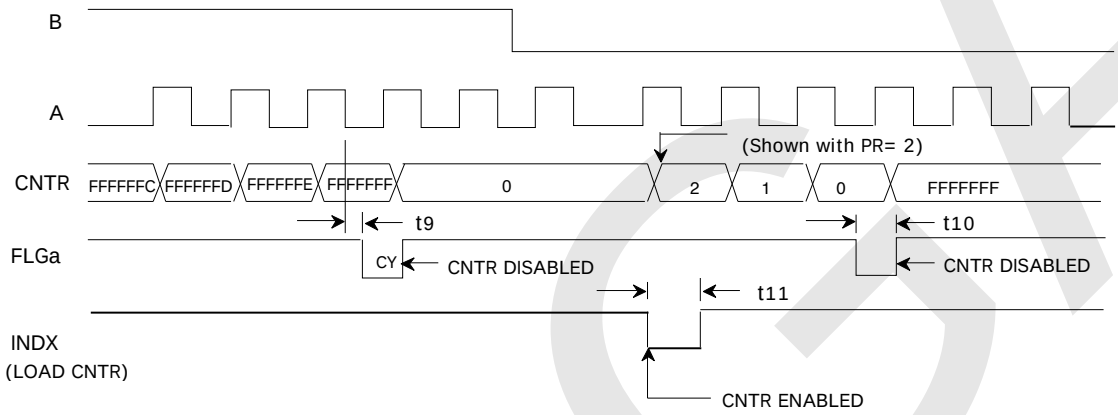


FIGURE 8. SINGLE-CYCLE, NON-QUADRATURE

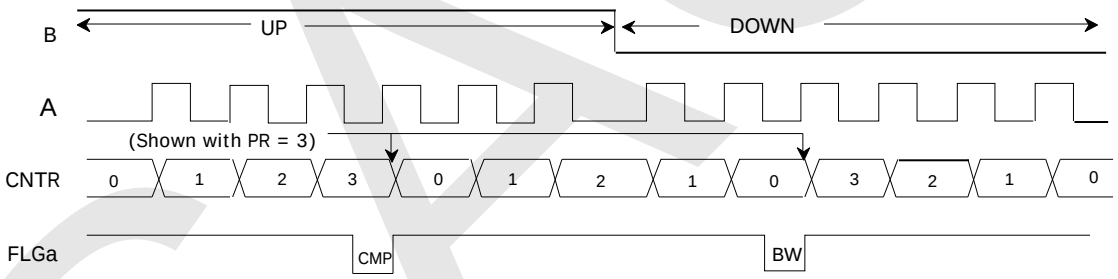


FIGURE 9. MODULO-N, NON-QUADRATURE

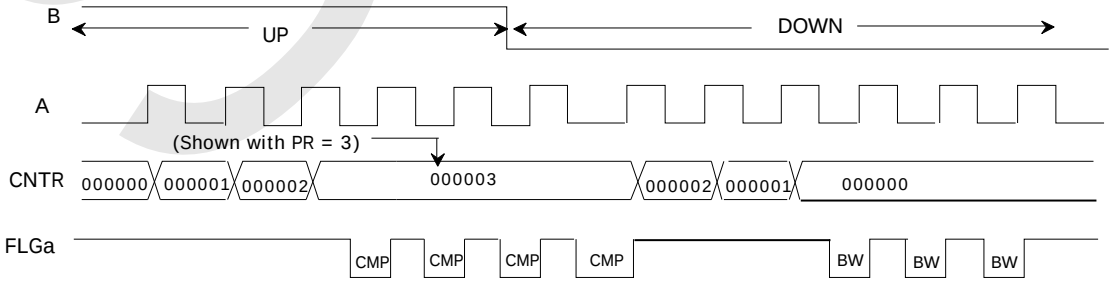


FIGURE 10. RANGE-LIMIT, NON-QUADRATURE

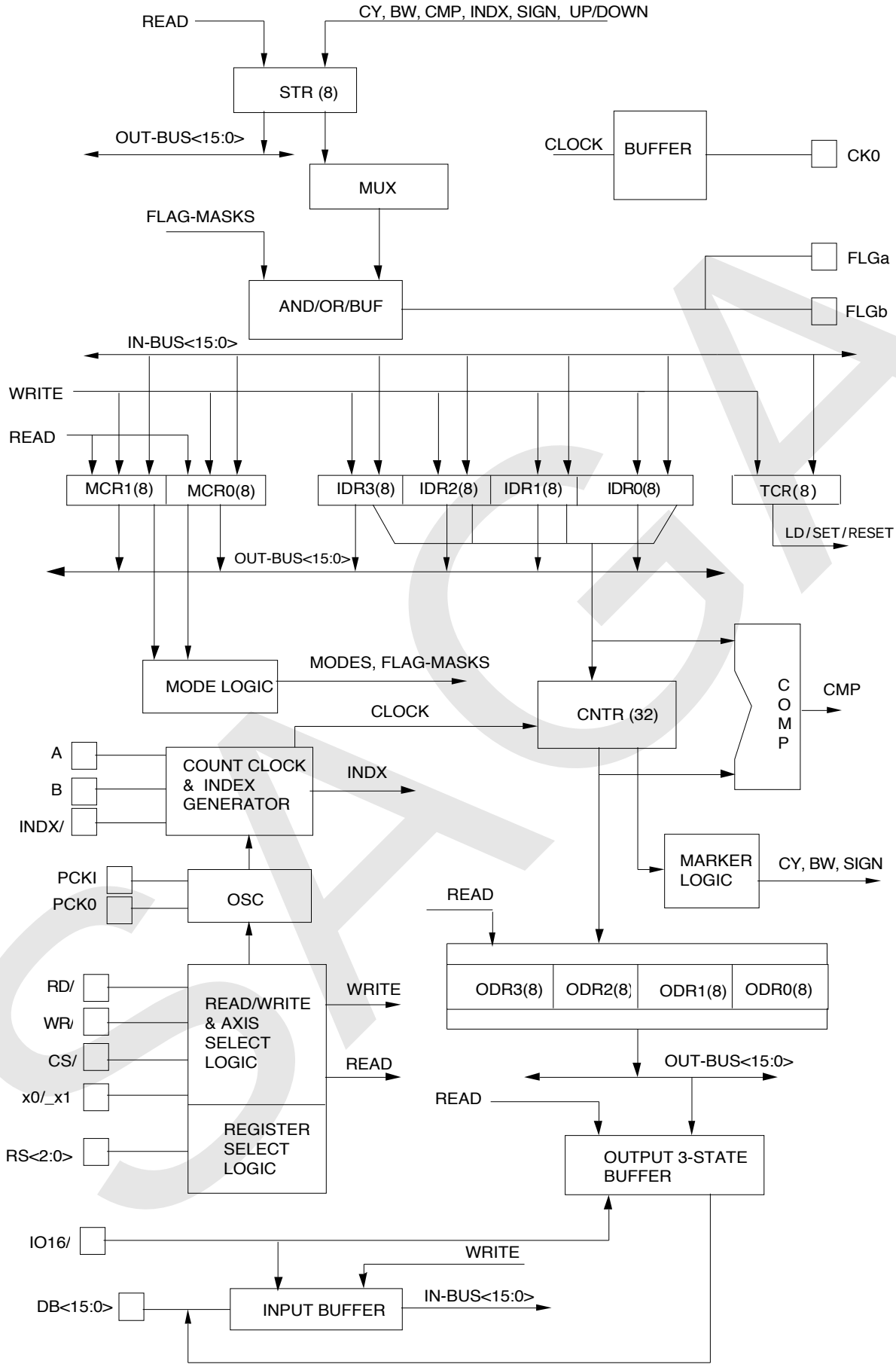


FIGURE 11. LS7766 BLOCK DIAGRAM FOR SINGLE-AXIS

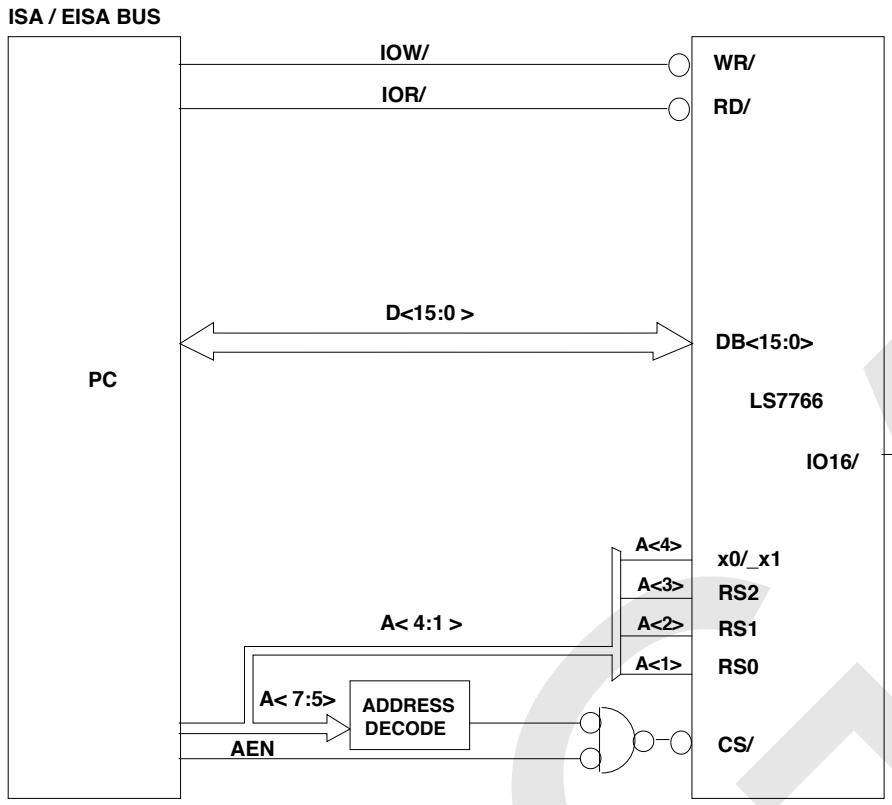


FIGURE 12. LS7766 TO ISA / EISA INTERFACE with 16-BIT BUS

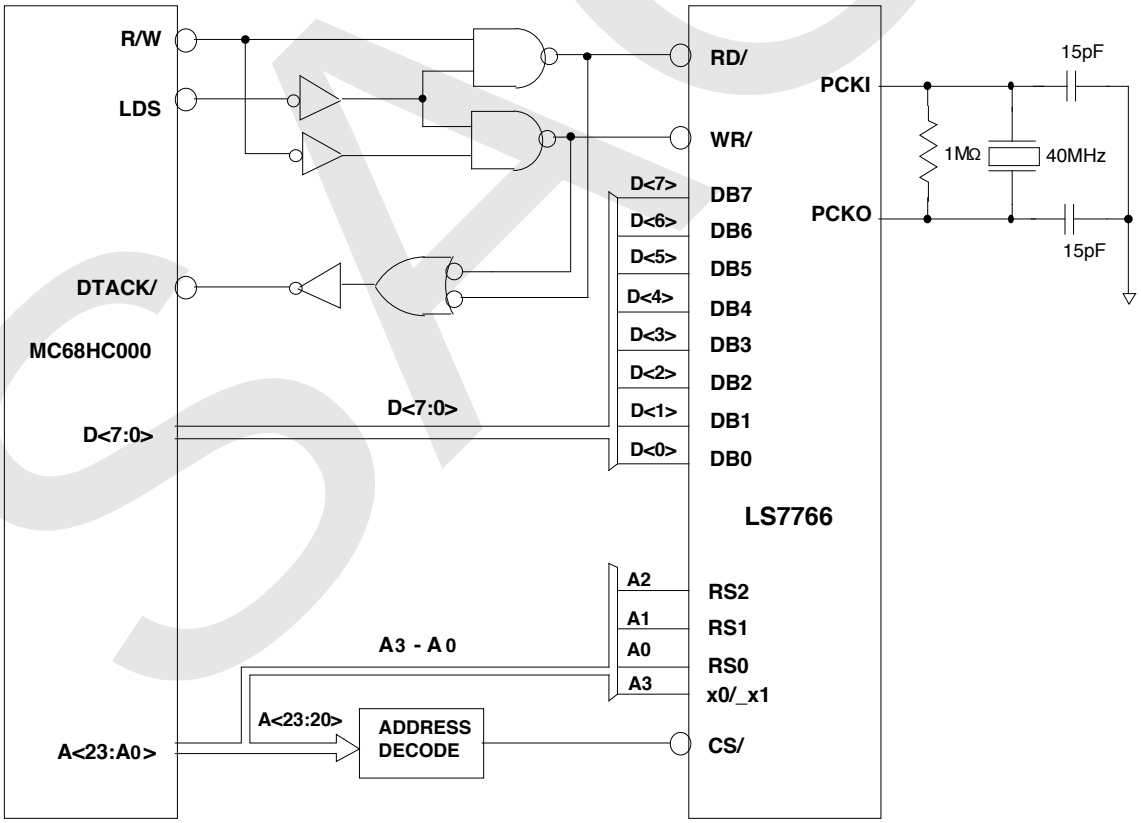


FIGURE 13. LS7766 TO MC68HC000 INTERFACE with 8-BIT BUS