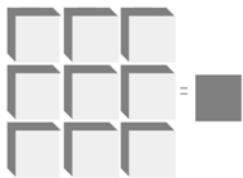


LSI/CSI



LS7273N



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30 VOLT QUAD-CHANNEL DIFFERENTIAL LINE DRIVER WITH OPEN DRAIN OUTPUTS

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FEATURES:

- Open-drain output drivers for return to power supply independent of VDD
- Voltage Range: 4.5V – 30V (V_{DD} – V_{SS})
- 120mA Sink/Source output drive
- Operating frequency up to 4 MHz
- Thermal shutdown protection for output driver overload
- Enable input with Thermal Shutdown disconnect feature
- 1.5A dynamic peak output current drive
- Outputs RS422A compatible
- Inputs CMOS/TTL compatible with hysteresis
- Output drivers fully connected or high-impedance state

PART NUMBER ORDERING INFORMATION:

This part is available in three package styles, DIP, SOIC, and TSSOP.

For DIP packages: LS7273N

For SOIC packages: LS7273N-S

For TSSOP packages: LS7273N-TS

PIN ASSIGNMENT – TOP VIEW

SI	1	VDD	16
A	2	D	15
AO	3	DO	14
n.c.	4	DO	13
BO	5	EN	12
BO	6	CO	11
B	7	CO	10
VSS	8	C	9

FIGURE 1

DESCRIPTION:

The LS7273N is a short-circuit proof Quad Differential Industrial Power Line Driver. It can operate up to 30V and have a selectable thermal shutdown features.

The Data inputs are TTL / CMOS compatible and can also be driven up to the supply voltage V_{DD}. The ENA input can be used to place all the outputs in a high impedance state.

The outputs are open drain and the loads can be returned to any voltage between 4.5V and 30V independent of V_{DD}.

An internal 5V regulated supply is used to power the logic and level converter blocks.

The thermal shutdown block located in the center of the IC can be disabled by setting the ENA input, Pin 12, to a voltage between 7.5V and 12V.

Upon power-up, a Power-On-Reset (POR) circuit block forces all output drivers to the high-impedance state until the power supply voltage reaches a nominal 3.8V. Included in the POR circuit block is a hysteresis of 100mV such that if the power supply drops below 3.7V all output drivers are forced to the high-impedance state until the voltage rises above 3.8V. There is a built-in 5μs delay for disabling the output drivers should the power supply drop below 3.7V. The output drivers are immediately enabled when the voltage rises above 3.8V.

INPUT / OUTPUT DESCRIPTION:

A / B / C / D

These are CMOS / TTL data inputs that can also operate with input levels up to the V_{DD} power supply. All data input blocks contain hysteresis.

AO / BO / CO / DO / \overline{AO} / \overline{BO} / \overline{CO} / \overline{DO}

These outputs are open-drain.

\overline{ENA}

A logic low on this CMOS / TTL compatible input enables the output drivers while logic high forces them into a high-impedance state. This input is also used to enable / disable the output short circuit thermal protection.

Applying a voltage between 7.5V and 12.5V to the \overline{ENA} input will disable the thermal shutdown protection function. When using this feature, the Line Driver Outputs are enabled but no longer protected.

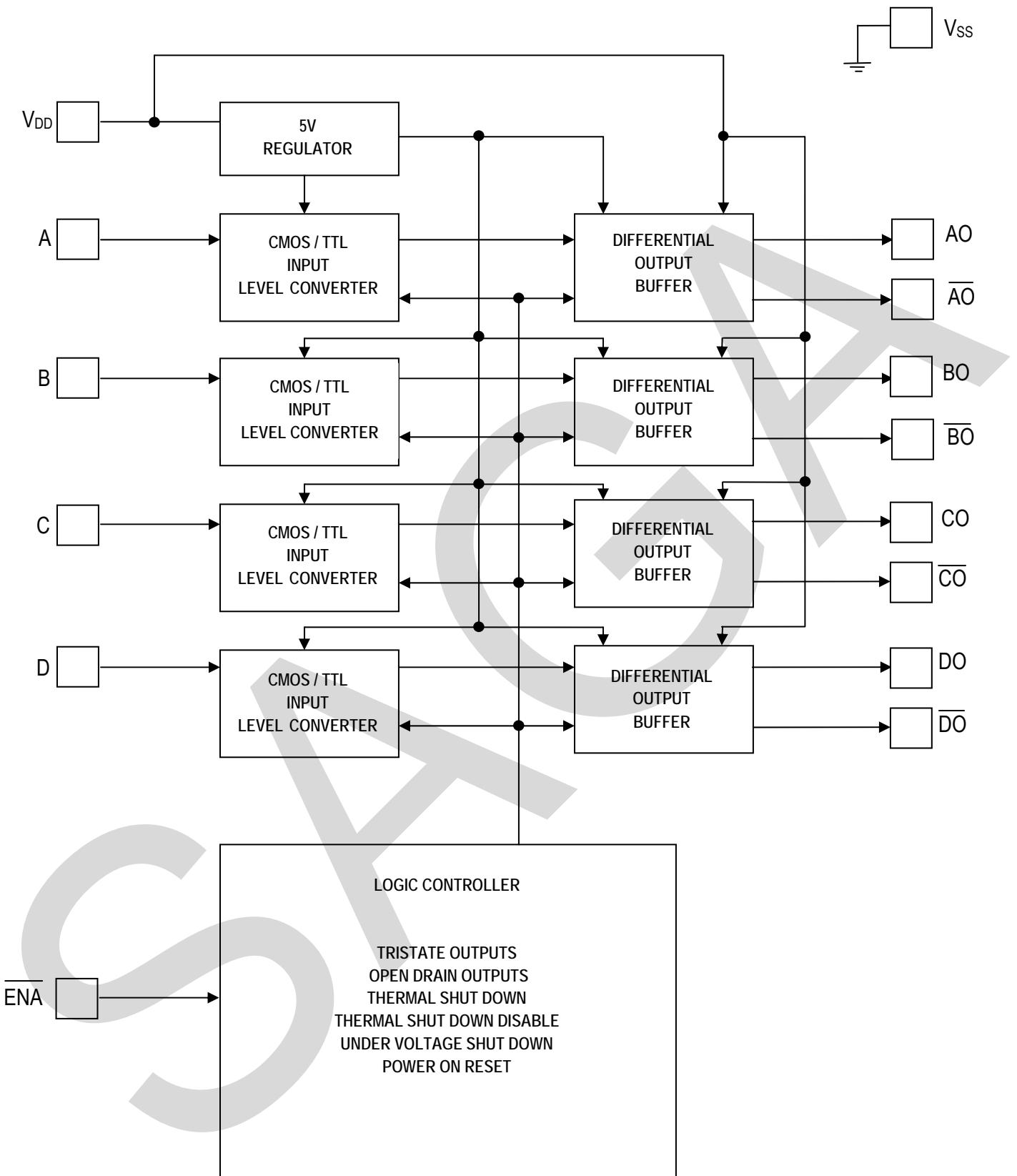


FIGURE 2 LS7273N BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	36	V
Data Output Voltage	V _{OUT}	4.5 to 36	V
Drive Output Current	I _{OUT}	1500 / 120	mA (pulse peak) / average
Data Input Voltage	V _{IND}	V _{DD} + 0.3	V
EN _A Input Voltage	V _{INE}	18	V
Operating Temperature	T _A	-55 to +125	°C
Storage Temperature	T _{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	4.5 to 30	V
Data Input Voltage	V _{IND}	0 to V _{DD}	V
EN _A Input Voltage	V _{INE}	0 to 5.5	V
Data Output Voltage	V _{OUT}	4.5 to 30	V
Data Output Current	I _{OUT}	100	mA
Operating Temperature	T _{OP}	-40 to +125	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Inputs:						
Data Input High-Threshold	V _{DH}	-	1.7	2.4	V	$\overline{\text{ENA}} \leq 0.8\text{V}$
Data Input Low Threshold	V _{DL}	0.8	1.2	-	V	$\overline{\text{ENA}} \leq 0.8\text{V}$
Data Input Hysteresis	V _{DHY}	-	0.5	-	V	$\overline{\text{ENA}} \leq 0.8\text{V}$
$\overline{\text{ENA}}$	V _{EH}	-	1.7	2.4	V	-
$\overline{\text{ENA}}$	V _{EL}	0.8	1.2	-	V	-
$\overline{\text{ENA}}$ Input Hysteresis	V _{EHY}	-	0.5	-	V	-
Inputs:						
Leakage Current	I _{LKG}	-5	+5	μA		
$\overline{\text{ENA}}$	I _{ESO}	-	100	μA		$\overline{\text{ENA}} = 12\text{V}$
Outputs:						
Output Resistance	R _{DSON}	-	20	-	Ω	$I_{\text{LOAD}} = 30\text{mA}$
Low Voltage Output Voltage	V _{OL}	-	0.3	-	V	$I_{\text{LOAD}} = -20\text{mA}, V_{\text{DD}} = 4.75\text{V}$
	V _{OL}	-	0.4	-	V	$I_{\text{LOAD}} = -30\text{mA}, V_{\text{DD}} = 30\text{V}$
High-Impedance Output						
Leakage Current (Outputs Disabled)	I _{OT}	-10	+10	μA		$V_{\text{DD}} = 20\text{V}, 2.4\text{V} < \overline{\text{ENA}} < 7.5\text{V}$
Reset:						
Power-On-Reset (POR)	V _{POR}	-	3.6	2.4	V	-
POR Hysteresis	V _{PORH}	-	0.1	-	V	-
POR Removal Time	T _{PORR}	-	5	-	μS	-
Over-Temperature Protection:						
Junction Temperature Operate Point	T _{JTO}	-	165	-	°C	
Junction Temperature Release Point	T _{JTR}	-	135	-	°C	
$\overline{\text{ENA}}$ Input Protection Inhibit	V _{EPI}	7.0	-	12.5	V	

NOTE: $\overline{\text{ENA}}$ input disables Outputs between 2.4V and 7.5V. $\overline{\text{ENA}}$ input enables Outputs between 7.5V and 12V but disables Temperature Shutdown. $\overline{\text{ENA}}$ input disables Outputs above 12V.

AC SWITCHING CHARACTERISTICS

(V_{DD} = 12V, TA = 25°C, Load Capacitance = 1000 pF)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Propagation delay from 50% point of input rising edge to zero crossing of differential outputs	T _{PLH}	-	105	150	ns	V _{DD} = 5V
		-	112	200	ns	V _{DD} = 12V
		-	135	250	ns	V _{DD} = 24V
Propagation delay from 50% point of input rising edge to zero crossing of differential outputs	T _{PHL}	-	105	150	ns	V _{DD} = 5V
		-	112	280	ns	V _{DD} = 12V
		-	135	330	ns	V _{DD} = 24V
Output Rise Time	T _R	-	*	-	-	-
Output Fall Time	T _F	-	65	125	ns	V _{DD} = 5V
		-	73	175	ns	V _{DD} = 12V
		-	101	250	ns	V _{DD} = 24V
ENA Enable Time	T _{ON}	-	60	200	ns	-
ENA Disable Time	T _{OFF}	-	80	200	ns	-

*Output rise time is a function of pull-up resistor and load capacitance.

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, or for any infringements of patent rights of others which may result from its use.